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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yeo, *et al.* Docket No.: TSM03-0556
Serial No.: 10/627,218 Art Unit: 2831
Filed: July 25, 2003 Examiner: TBD
For: Capacitor With Enhanced Performance and Method of Manufacture

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Form PTO/SB/08A & 08B with 59 References Cited (5 pages)
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Respectfully submitted,

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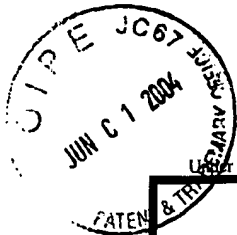
No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits. If any fee is required, please charge any additional amount, or credit any overpayment to Deposit Acct. No 50-1065 of the below mentioned firm.

Respectfully submitted,

May 26, 2004
Date


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Substitute for form 1449/PTO			Complete if Known		
			Application Number	10/627,218	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Filing Date	July 25, 2003	
			First Named Inventor	Yeo, et al.	
			Art Unit	2831	
			Examiner Name	TBD	
Sheet	1	of	5	Attorney Docket Number	TSM03-0556

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	1	US-4,314,269	02-02-1982	Fujiki	
	2	US-4,631,803	12-30-1986	Hunter, et al.	
	3	US-4,946,799	08-07-1990	Blake, et al.	
	4	US-5,447,884	09-05-1995	Fahey, et al.	
	5	US-5,461,250	10-24-1995	Burghartz, et al.	
	6	US-5,534,713	07-09-1996	Ismail, et al.	
	7	US-5,629,544	05-13-1997	Voldman, et al.	
	8	US-5,714,777	02-03-1998	Ismail, et al.	
	9	US-5,763,315	06-09-1998	Benedict, et al.	
	10	US-5,811,857	09-22-1998	Assaderaghi, et al.	
	11	US-6,008,095	12-28-1999	Gardner, et al.	
	12	US-6,015,993	01-18-2000	Voldman, et al.	
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	18	US-6,294,834 B1	09-25-2001	Yeh, et al.	
	19	US-6,387,739 B1	05-14-2002	Smith, III	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/627,218
				Filing Date	July 25, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Art Unit	2831
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0556
Sheet	2	of	5		

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				Filing Date	July 25, 2003
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				Examiner Name	TBD
Sheet	3	of	5	Attorney Docket Number	TSM03-0556

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cita. No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	32	ISMAIL, K, <i>et al.</i> , "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.	
	33	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.	
	34	GAMIZ, F., <i>et al.</i> , "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.	
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	41	TIWARI, S., <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp. 939-941.	
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Examiner Signature			Date Considered

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Sheet	4	of	5	Attorney Docket Number	TSM03-0556

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	45	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers -- III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	46	SCHÜPPEN, A., <i>et al.</i> , "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
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	55	WELSER, J., <i>et al.</i> , "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.	
	56	BLAAUW, D., <i>et al.</i> , "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.	
	57	"Future Gate Stack," International Sematech, 2001 Annual Report.	
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Sheet	5	of	5		

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